REMARKS

Claims 1-18 are pending in this application. In this Amendment, claims 1, 7, 13 and 17 have been amended to improve wording. Care has been exercised to avoid the introduction of new matter.

Information Disclosure Statement.

Applicant notes that the Information Disclosure Statement filed July 25, 2001 has not been acknowledged. Applicant respectfully requests the Examiner to clarify the record by acknowledging receipt of the IDS and provide a copy of the PTO-1449 form appropriately initialed indicating consideration of the cited prior art.

The drawings has been objected.

The Examiner asserted that Fig. 1 does not show a conventional data processing device 500 which is referred to on page 1, line 28 and lines 32-33 of the specification. In response, Applicant has amended the specification to delete reference numeral 500, instead of amending Fig. 1. Withdrawal of the objection is respectfully solicited.

The specification has been objected.

It has been pointed out that the description refers to incorrect or non-existent items in the drawings. In response, the relevant portion of the specification has been amended thereby overcoming the stated bases for the objection to the specification.

The Examiner also requested a new title of the invention. In response, the title has been amended to "Data Processing Device with Instruction Translator and Memory Interface Device to Translate Non-Native Instructions into Native Instructions for Processor."

Therefore, Applicant respectfully solicits withdrawal of the objection to the specification.

Claims 1-16 have been objected.

The Examiner asserted that the phrase "said data being an instruction nonnatives to said processor" includes an error. In response, the word "nonnatives" in the phase has been amended to --nonnative--. Withdrawal of the objection to the claims is respectfully solicited.

Claims 1, 7 and 13 have been rejected under 35 U.S.C. §102(e) as being anticipated by Augusteijn et al.

In the statement of the rejection, the Examiner asserted that Augusteijn et al. discloses converting program-specific virtual machine instructions into variable instruction set identically corresponding to what is claimed. This rejection is respectfully traversed.

It is well established precedent that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *See EMI Group N. Am., Inc. v. Cypress Semiconductor Corp.*, 268 F.3d 1342, 60 USPQ2d 1423 (Fed. Cir. 2001); *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

Applicant submits that Augusteijn et al. does not disclose the claimed invention recited in independent claims1, 7 and 13. Specifically, the reference does not disclose "selectively applying the data read from said external memory space and the instruction prepared by the translation of the instruction read from said external memory space to said processor core depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not," recited in claims 1, 7 and 13 (emphasis added).

Augusteijn et al. discloses converting program-specific virtual machine instructions into native instruction of a core (see the Abstract). However, the Examiner's cited portions in Augusteijn et al. merely describes selecting native instructions or instructions converted from non-native instructions (see column 10, lines 36-56; and column 5, line 64 to column 6, line 8 of Augusteijn et al.). Therefore, it is apparent that Augusteijn does not disclose, and the Examiner did not point out where the reference disclose, conditions to select the native instructions or the converted instructions, as recited in the claims, i.e., "depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not."

Since Augusteijn et al. does not at least disclose how to select native instructions or instructions converted from non-native instructions, Applicant submits that the imposed rejection of claims 1, 7 and 13 under 35 U.S.C. §102(e) for lack of novelty as evidenced by Augusteijn et al. is not factually viable and, hence, respectfully solicits withdrawal thereof.

Claims 1, 7 and 13 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Arya in view of Hammond et al.

In the statement of the rejection, the Examiner admitted that Arya does not teach "selectively applying... depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not," recited in claims 1, 7 and 13 (emphasis added). However, the Examiner asserted that Hammond et al. teaches such limitation by relying upon a selector circuit (demultiplexer) 540 shown in Fig. 5 of the reference. This rejection is respectfully traversed.

Applicant submits that the Examiner has not established a *prima facie* basis to deny patentability to the claimed invention under 35 U.S.C. §103 for lack of the requisite factual basis. To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Arya and Hammond et al., either individually or in combination, do not teach each and every limitation of claims 1, 7 and 13.

Arya discloses a hardware compatibility circuit for a new processor architecture, and Hammond et al. discloses a processor capable of executing programs that contain RISC and CISC instructions. As admitted by the Examiner, Arya does not teach "selectively applying... depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not," recited in claims 1, 7 and 13. Although the Examiner asserted that selector circuit (demultiplexer) 540 of Hammond et al. corresponds to the above limitation, Applicant does not respectfully disagree with the Examiner. The following is reproduction of column 14, line 67 to column 15, line 6 of Hammond et al.

> The selection of demultiplexer 540 is based on the signal received by demultiplexer 540 from decoder 543. The first signal from decoder 543 causes demultiplexer 540 to select translator 541 and the first instruction set mode. A second signal from decoder 543 causes demultiplexer 540 to select instruction cache 542 and the second instruction set mode (emphasis added).

It is apparent that Hammond et al. does not teach causing demultiplexer 540 to select translator 541 or instruction cache 520 depending on whether the address value for the access from said processor core to said external memory space is in a predetermined region or not. Hammond et al. merely describes selecting translator 541 and the first instruction set mode when the first signal from decoder 543 is received, and selecting the instruction cache 542 and the second instruction mode when the second signal is received. This description does not suggest the condition "whether the address value for the access from said processor core to said external memory space is in a predetermined region or not," recited in claims 1, 7 and 13.

Thus, consideration of the teachings of Arya and Hammond et al., either individually or in combination, do not teach each and every limitation of claims 1, 7 and 13. In the instant case, the pending rejection has not established *prima facie* obviousness of the claimed invention as recited in claims 1, 7 and 13, because the proposed combination fails to teach all the claim limitations within the meaning of 35 U.S.C. §103. Applicant, therefore, solicits withdrawal of the rejection of claims 1, 7 and 13.

Claims 2-4, 8-10 and 14-16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Augusteijn et al. in view of IBM Technical Disclosure Bulletin, NN610843 ("IBM TDB"); claims 5, 11 and 17 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Arya in view of Hammond et al. and further in view of Denman; and claims 6, 12 and 18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Arya in view of Hammond et al. and further in view of Jouppi.

Based on the forgoing, Applicant submits that dependent claims 2-6, 8-12 and 14-18 are patentably distinguishable at least because they include all the limitations recited in independent claims 1, 7 and 13, respectively. That is, the applied combinations do not teach or suggest all the

limitations recited in independent claims 1, 7 and 13. IBM TDB, Denman, and Jouppi do not cure deficiencies of Augusteijn et al., and the applied combination of Arya and Hammond et al. Accordingly, Applicant respectfully solicits withdrawal of the rejection of the claims and favorable consideration thereof.

Conclusion.

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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